AMENDMENTS TO THE SPECIFICATION

Please amend the specification as indicated hereafter to correct minor typographical errors. It is believed that the following amendments and additions add no new matter to the present application.

Please replace the paragraph starting on p. 12, line 6 with the following amended paragraph:

The JO JTAG register 164 is connected to the JT JTAG register 162 and the JI JTAG register 166 via the boundary-scan chain 114. In addition, the ~~JO TAG~~ JO JTAG register 164 is connected to an input of the driver circuit 152 for providing the driver circuit 152 with serial data utilized for testing the IC 102. The JI JTAG register 166 is connected to the JO JTAG register 164 and an output of the pad 104 via the boundary-scan chain 114. As mentioned above, the boundary-scan chain 114 is also connected to other pads 104. The JI JTAG register 166 is also connected to an output of the receiver circuit 154. An output of the driver circuit 152 and an input of the receiver circuit 154 are connected to each other, as well as being connected to an I/O pin 106 (FIG. 2).

Please replace the paragraph starting on p. 13, line 16 with the following amended paragraph:

FIG. 4 is a flow chart that shows the architecture, functionality, and operation of a possible implementation of the present data generating system ~~100~~ that automates the process of creating the BSDL file. In this regard, each block represents a module, segment, or portion of code, which comprises one or more executable instructions for implementing the specified logical function(s). It should also be noted that in some alternative implementations, the functions noted in the blocks may occur out of the order noted. For example, two blocks shown in succession may in fact be executed

substantially concurrently or the blocks may sometimes be executed in the reverse order, depending upon the functionality involved, as will be further clarified herein below.

Please replace the paragraph starting on p. 16, line 3 with the following amended paragraph:

Since description of the JO JTAG 164 requires a description of the driver circuit 152, which is tri-stated by the JT JTAG register 162, a description of the JT JTAG register 162 is also required. Therefore, the flat netlist is traversed from an output of the JT JTAG register 162 to the driver circuit 152 and continued until an I/O pin 106 is located ~~106~~. The path from the output of the JT JTAG register 162 to the I/O pin 106 is stored for use in creating the BSDL file.